--22. An image processing system as set forth in claim 21, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and generates the sequence of input words into the first memory in response to the line of frame buffered display information accessed by the accessing circuit.

--23. An image processing system as set forth in claim 21, further comprising:

a kernel memory coupled to the first output circuit and to the second output circuit and storing a kernel of output words in response to the first sequence of output words generated by the first output circuit and in response to the second sequence of output words generated by the second output circuit; and

a kernel processor coupled to the kernel memory and generating a sequence of spatially filtered output words in response to the kernel of display information stored by the kernel memory.

--24. An image processing system as set forth in claim 23, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the spatially filtered output words.

--25. An image processing system as set forth in claim 21, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the writing of the sequence of input words into the first memory by the input circuit is at a first word rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal, wherein the outputting of the first sequence of output words from the second memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal and wherein the outputting of the second sequence of output words from the third memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal.

--26. An image processing system comprising:

a processor generating rotated image information;

a plurality of memories storing words of information;

an input circuit generating a sequence of input words in response to the image information;

a first buffer coupled to the plurality of memories and to the input circuit and writing a sequence of input words into at least one of the memories included in the plurality of memories in response to the sequence of input words;

a second buffer coupled to the plurality of memories and accessing a sequence of words of information from each of at least two of the memories included in the plurality of memories;

an output circuit coupled to the second buffer and outputting a plurality of sequences of output words in response to the words of information accessed from the at least two of the memories included in the plurality of memories;

a double buffer control circuit generating a double buffer control signal; and

a double buffer selection circuit coupled to the double buffer control circuit, to the first buffer, and to the second buffer and selecting the memory for the first buffer and selecting the at least two of the memories for the second buffer in response to the double buffer control signal.

--27. An image processing system as set forth in claim 21, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and generates the sequence of input words in response to the line of frame buffered display information accessed by the accessing circuit.

--28. An image processing system as set forth in claim 21, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of output words in response to the plurality of sequences of output words; and

a kernel processor coupled to the kernel memory and generating a sequence of spatially filtered output words in response to the kernel of output words stored by the kernel memory.

--29. An image processing system as set forth in claim 23, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the spatially filtered output words.

--30. An image processing system as set forth in claim 21, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the generating of the sequence of input words is at a first word rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal,

wherein the outputting of the plurality of sequences of output words is at a higher word rate than the first word rate in response to the second clock signal.

--31. An image processing system comprising:

a processor generating translated image information;

a plurality of memories including a first memory, a second memory, a third memory, and a forth memory;

an input circuit coupled to the first memory and writing a sequence of input words into the first memory in response to the image information; and

an output circuit coupled to the second memory, to the third memory and to the forth memory and outputting a first sequence of output words from the second memory, outputting a second sequence of output words from the third memory, and outputting a third sequence of output words from the forth memory simultaneously with the writing of the sequence of input words into the first memory by the input circuit.

--32. An image processing system as set forth in claim 26, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and writes the sequence of input words into the first memory in response to the line of frame buffered display information accessed by the accessing circuit.

--33. An image processing system as set forth in claim 26, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of output words in response to the first sequence of output words, in response to the second sequence of

output words, and in response to the third sequence of output words; and

a kernel processor coupled to the kernel memory and generating a sequence of spatially filtered output words in response to the kernel of output words stored by the kernel memory.

--34. An image processing system as set forth in claim 28, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the spatially filtered output words.

--35. An image processing system as set forth in claim 26, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the writing of the sequence of input words into the first memory by the input circuit is at a first word rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal, wherein the outputting of the first sequence of output words from the second memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal; wherein the second sequence of output words from the third memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal; and wherein the outputting of the third sequence of output words from the forth memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal.

--36. An image processing system comprising:

a processor generating scaled image information;

a plurality of memories including a first memory, a second memory, a third memory, and a forth memory;

an input circuit coupled to the first memory and storing a sequence of input words into the first memory in response to the image information;

an output circuit coupled to the second memory, to the third memory and to the forth memory and outputting a first sequence of output words from the second memory, outputting a second sequence of output words from the third memory, and outputting a third sequence of output words from the forth memory simultaneously with the storing of the sequence of input words into the first memory by the input circuit; and

a kernel processor coupled to the second memory, the third memory, and the forth memory and generating a filtered sequence of output words by kernel processing the first sequence of output words, the second sequence of output words, and the third sequence of output words.

--37. An image processing system comprising:

a processor generating perspective image information;

a plurality of memories including a first memory, a second memory, and a third memory;

a first selection circuit coupled to the first memory, the second memory, and the third memory and selecting either the first memory, the second memory, or the third memory as an input memory;

an input circuit coupled to the input memory and storing a sequence of input words into the input memory in response to the image information;

a second selection circuit coupled to the first memory, the second memory, and the third memory and selecting either the first memory, the second memory, or the third memory as a first output memory;

a third selection circuit coupled to the first memory, the second memory, and the third memory and selecting either the first memory, the second memory, or the third memory as a second output memory; and

an output circuit coupled to the first output memory and to the second output memory and outputting a first sequence of output words from the first output memory and a second sequence of output words from the second output memory.

--38. An image processing system as set forth in claim 32, wherein the output circuit is a simultaneous output circuit and outputting the first sequence of output words from the first output memory and the second sequence of output words from the second output memory simultaneously with the storing of the sequence of input words into the input memory by the input circuit.

--39. An image processing system as set forth in claim 32, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and storing the sequence of input words into the input memory in response to the line of frame buffered display information accessed by the accessing circuit.

--40. An image processing system as set forth in claim 32, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of output words in response to the first sequence of output words and in response to the second sequence of output words; and

a kernel processor coupled to the kernel memory and generating a sequence of spatially filtered output words in response to the kernel of display information stored by the kernel memory.

--41. An image processing system as set forth in claim 35, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the spatially filtered output words.

--42. An image processing system as set forth in claim 32, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the storing of the sequence of input words into the input memory by the input circuit is at a first word rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal, wherein the outputting of the first sequence of output words from the first output memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal and wherein the outputting of the second sequence of output words from the second output memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal.

--43. An image processing system as set forth in claim 32, further comprising a kernel processor coupled to the output circuit and processing a kernel of words in response to the first sequence of output words from the first output memory and the second sequence of output words from the second output memory.

--44. An image processing system as set forth in claim 32, wherein the input circuit is a display input circuit storing the sequence of input words as a sequence of display pixel input words into the input memory and wherein the output circuit is a display output circuit outputting the first sequence of output words as a first sequence of display pixel output words from the

first output memory and outputting the second sequence of output words as a second sequence of display pixel output words from the second output memory.

--45. An image processing system as set forth in claim 32, further comprising a kernel processor coupled to the display output circuit and processing a kernel of display pixel words in response to the first sequence of display pixel words from the first output memory and in response to the second sequence of display pixel words from the second output memory.

--46. An image processing system comprising:

a processor generating antialiased image information;

an input circuit generating an input line of display information in response to the image information;

a triple line buffer coupled to the input circuit and storing three lines of display information in response to the input line of display information generated by the input circuit; and

an output circuit coupled to the double buffered triple line buffer and simultaneously generating three lines of display information in response to the three lines of double buffered display information stored by the double buffered triple line buffer.

--47. An image processing system as set forth in claim 41, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and generates the input line of display information in response to the line of frame buffered display information accessed by the accessing circuit.

--48. An image processing system as set forth in claim 41, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of display information in response to the three lines of display information generated by the output circuit; and

a kernel processor coupled to the kernel memory and generating a line of spatially filtered display information in response to the kernel of display information stored by the kernel memory.

--49. An image processing system as set forth in claim 43, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the line of spatially filtered display information.

--50. An image processing system as set forth in claim 41, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the generating of the input line of display information by the input circuit is at a first information rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first clock rate of the first clock signal, wherein the generating of the three lines of display information by the output circuit is at a higher information rate than the first information rate in response to the second clock signal.

--51. An image processing system comprising:

a processor generating scanned out image information;

an input circuit generating an input line of display information in response to the image information;

a double buffered triple line buffer coupled to the input circuit and storing three lines of double buffered display

information in response to the input line of display information generated by the input circuit; and

an output circuit coupled to the double buffered triple line buffer and simultaneously generating three lines of display information in response to the three lines of double buffered display information stored by the double buffered triple line buffer.

--52. An image processing system comprising:

a processor generating filtered image information;

an input circuit generating an input line of display information in response to the image information;

a double buffered triple line buffer coupled to the input circuit and storing three lines of double buffered display information in response to the input line of display information generated by the input circuit; and

an output circuit coupled to the double buffered triple line buffer and simultaneously generating three lines of display information in response to the three lines of double buffered display information stored by the double buffered triple line buffer.

--53. An image processing system as set forth in claim 47, wherein the double buffered triple line buffer is implemented with no more than four line buffers storing the three lines of double buffered display information.

--54. An image processing system as set forth in claim 47, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and

generates the input line of display information in response to the line of frame buffered display information accessed by the accessing circuit.

--55. An image processing system as set forth in claim 47, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of display information in response to the three lines of display information simultaneously generated by the output circuit; and

a kernel processor coupled to the kernel memory and generating a line of spatially filtered display information in response to the kernel of display information stored by the kernel memory.

--56. An image processing system as set forth in claim 47, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the spatially filtered display information.

--57. An image processing system as set forth in claim ~~16~~ 52, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the generating of the input line of display information by the input circuit is at a first information rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal, wherein the generating of the three lines of display information by the output circuit is at a higher information rate than the first information rate in response to the second clock signal.

--58. An image processing system comprising:

a processor generating occulted image information;

an input circuit generating an input line of display information in response to the image information;

a first line buffer coupled to the input circuit and storing a first line of display information in response to the input line of display information generated by the input circuit;

a first accessing circuit coupled to the first line buffer and accessing the first line of display information stored by the first line buffer;

a second line buffer coupled to the first accessing circuit and storing a second line of display information in response to the first line of display information accessed by the first accessing circuit from the first line buffer; and

a second accessing circuit coupled to the second line buffer and accessing the second line of display information stored by the second line buffer.

--59. An image processing system as set forth in claim 53, further comprising a kernel processor coupled to the input circuit, to the first accessing circuit, and to the second accessing circuit and generating a filtered line of display information in response to the input line of display information generated by the input circuit, in response to the first line of display information accessed by the first accessing circuit from the first line buffer, and in response to the second line of display information accessed by the second accessing circuit from the second line buffer.

--60. An image processing system comprising:

a processor generating range-related detail image information;

an input circuit generating an input line of display information in response to the image information;

a first line buffer coupled to the input circuit and storing a first line of display information in response to the

input line of display information generated by the input circuit;

a first accessing circuit coupled to the first line buffer and accessing the first line of display information stored by the first line buffer;

a second line buffer coupled to the first accessing circuit and storing a second line of display information in response to the first line of display information accessed by the first accessing circuit from the first line buffer;

a second accessing circuit coupled to the second line buffer and accessing the second line of display information stored by the second line buffer;

a third line buffer coupled to the second accessing circuit and storing a third line of display information in response to the second line of display information accessed by the second accessing circuit from the second line buffer; and

a third accessing circuit coupled to the third line buffer and accessing the third line of display information stored by the third line buffer.

--61. An image processing system as set forth in claim 55, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and generates the input line of display information in response to the line of frame buffered display information accessed by the accessing circuit.

--62. An image processing system as set forth in claim 55, further comprising a kernel processor coupled to the first accessing circuit, to the second accessing circuit, and to the third accessing circuit and generating a filtered line of display information in response to the first line of display information accessed by the first accessing circuit from the first line

buffer, in response to the second line of display information accessed by the second accessing circuit from the second line buffer, and in response to the third line of display information accessed by the third accessing circuit from the third line buffer.

--63. An image processing system as set forth in claim 57, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the filtered line of display information generated by the kernel processor.

--64. An image processing system as set forth in claim 55, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the generating of the input line of display information by the input circuit is at a first information rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal; wherein the first line of display information accessed by the first accessing circuit is at a higher information rate than the first information rate in response to the second clock signal, the second line of display information accessed by the second accessing circuit is at a higher information rate than the first information rate in response to the second clock signal, and the third line of display information accessed by the third accessing circuit is at a higher information rate than the first information rate in response to the second clock signal.

--65. An image processing system comprising:

a processor generating image information;

an input circuit generating an input sequence of words in response to the image information;

a plurality of memories each storing a sequence of words;

an output circuit generating a plurality of simultaneous output sequences of words;

a precessing circuit coupled to the input circuit, to the output circuit, and to the plurality of memories and precessing the plurality of memories between an input memory storing the input sequence of words and a plurality of output memories each generating a sequence of words simultaneously with the other output memories each generating a sequence of words.

--66. An image processing system as set forth in claim 60, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and generates the input sequence words in response to the line of frame buffered display information accessed by the accessing circuit.

--67. An image processing system as set forth in claim 60, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of words in response to the plurality of simultaneous output sequences of words; and

a kernel processor coupled to the kernel memory and generating a sequence of spatially filtered output words in response to the kernel of words stored by the kernel memory.

--68. An image processing system as set forth in claim 62, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the sequence of spatially filtered output words.

--69. An image processing system as set forth in claim 60, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the generating of the input sequence of words by the input circuit is at a first word rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal, wherein the generating of the plurality of simultaneous output sequences of words by the output circuit is at a higher word rate than the first word rate in response to the second clock signal.

--70. An image processing system comprising:

a processor generating rotated image information;

an input circuit generating input words in response to the image information;

an output circuit generating output words;

a plurality of random access memories each storing words;

a first address generator generating a first address;

a second address generator generating a second address;

an address multiplexer circuit coupled to the first address generator and to the second address generator and multiplexing the first address and the second address to provide the first address to at least one of the plurality of random access memories and to provide the second address to at least one of the plurality of random access memories in response to an address control signal;

an input multiplexer circuit coupled to the input circuit and to the plurality of random access memories and selecting at least one of the random access memories that is to receive the input words generated by the input circuit in response to an input control signal;

an output multiplexer circuit coupled to the output circuit and to the plurality of random access memories and selecting at least one of the random access memories that is to provide the output words to the output circuit in response to an output control signal;

a control circuit coupled to the address multiplexer circuit, to the input multiplexer circuit, and to the output multiplexer circuit and generating the address control signal, the input control signal, and the output control signal to select at least one input memory storing the input words and at least one output memory generating the output words.

--71. An image processing system as set forth in claim 65, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and generates the input words in response to the line of frame buffered display information accessed by the accessing circuit.

--72. An image processing system as set forth in claim 65, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of output words in response to the plurality of simultaneous output sequences of words generated by the output circuit; and

a kernel processor coupled to the kernel memory and generating a sequence of spatially filtered output words in response to the kernel of output words stored by the kernel memory.

--73. An image processing system as set forth in claim 67, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the sequence of spatially filtered output words.

--74. An image processing system as set forth in claim 65, further comprising:

a first clock circuit coupled to the first address generator and generating a first clock signal having a first clock rate, wherein the generating of the first address by the first address generator is at a first address rate in response to the first clock signal and

a second clock circuit coupled to the second address generator and generating a second clock signal having a second clock rate that is higher than the first clock rate of the first clock signal, wherein the generating of the second address by the second address generator is at a second address rate in response to the second clock signal and wherein the second address rate is higher than the first address rate.

--75. An image processing system comprising:

a processor generating translated image information;

an input circuit generating an input sequence of words in response to the image information;

an output circuit generating a plurality of simultaneous output sequences of words;

a plurality of random access memories each storing a sequence of words;

an input address generator generating an input address;

an output address generator generating an output address;

an address multiplexer circuit coupled to the input address generator and to the output address generator and multiplexing the input address and the output address to provide the input address to an input one of the plurality of random access memories and to provide the output address to a plurality

of output ones of the plurality of random access memories in response to an address precessional control signal;

an input multiplexer circuit coupled to the input circuit and to the plurality of random access memories and selecting the random access memory that is to receive the input sequence of words generated by the input circuit in response to an input precessional control signal;

an output multiplexer circuit coupled to the output circuit and to the plurality of random access memories and selecting the plurality of random access memories that are to generate an output sequences of words to the output circuit in response to an output precessional control signal;

a precessing circuit coupled to the address multiplexer circuit, to the input multiplexer circuit, and to the output multiplexer circuit and generating the address precessional control signal, the input precessional control signal, and the output precessional control signal to precess the plurality of memories between an input memory storing the input sequence of words and a plurality of output memories each generating a sequence of words simultaneously with the other output memories each generating a sequence of words.

--76. An image processing system as set forth in claim 70, further comprising:

a frame buffer storing a frame of display information; and

an accessing circuit coupled to the frame buffer and accessing a line of frame buffered display information, wherein the input circuit is coupled to the accessing circuit and generates the input sequence of words in response to the line of frame buffered display information accessed by the accessing circuit.

--77. An image processing system as set forth in claim 70, further comprising:

a kernel memory coupled to the output circuit and storing a kernel of output words in response to the plurality of simultaneous output sequences of words generated by the output circuit; and

a kernel processor coupled to the kernel memory and generating a sequence of spatially filtered output words in response to the kernel of display information stored by the kernel memory.

--78. An image processing system as set forth in claim 72, further comprising a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the spatially filtered output words.

--79. An image processing system as set forth in claim 70, further comprising:

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the generating of the input sequence of words by the input circuit is at a first word rate in response to the first clock signal; and

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal, wherein the generating of the plurality of simultaneous output sequences of words by the output circuit is at a higher word rate than the first word rate in response to the second clock signal.

--80. An image processing system comprising:

a processor generating scaled image information;

a frame buffer storing a frame of display information in response to the image information;

an accessing circuit coupled to the frame buffer and accessing a line of display information;

a double buffered triple line buffer implemented with four line buffers, wherein the double buffered triple line buffer

includes a display line digital random access first memory, a display line digital random access second memory, a display line digital random access third memory, and a display line digital random access forth memory;

an input circuit coupled to the first memory and writing a sequence of input words into the first memory, each input word having 3 color nibbles of 3 bits each nibble, wherein the input circuit is coupled to the accessing circuit and generates the sequence of input words into the first memory in response to the line of display information accessed by the accessing circuit;

a first output circuit coupled to the second memory and outputting a first sequence of output words, each output word having 3 color nibbles of 3 bits each nibble, from the second memory simultaneously with the writing of the sequence of input words into the first memory by the input circuit;

a second output circuit coupled to the third memory and outputting a second sequence of output words, each output word having 3 color nibbles of 3 bits each nibble, from the third memory simultaneously with the writing of the sequence of input words into the first memory by the input circuit and simultaneously with the outputting of the first sequence of output words from the second memory by the first output circuit;

a third output circuit coupled to the forth memory and outputting a third sequence of output words, each output word having 3 color nibbles of 3 bits each nibble, from the forth memory simultaneously with the writing of the sequence of input words into the first memory by the input circuit, simultaneously with the outputting of the first sequence of output words from the second memory by the first output circuit, and simultaneously with the outputting of the second sequence of output words from the third memory by the second output circuit;

a first clock circuit coupled to the input circuit and generating a first clock signal having a first clock rate, wherein the writing of the sequence of input words into the first

memory by the input circuit is at a first word rate in response to the first clock signal;

a second clock circuit coupled to the output circuit and generating a second clock signal having a second clock rate that is higher than the first rate of the first clock signal, wherein the outputting of the first sequence of output words from the second memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal, wherein the outputting of the second sequence of output words from the third memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal, and wherein the outputting of the third sequence of output words from the fourth memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal;

a kernel memory coupled to the first output circuit, the second output circuit, and the third output circuit and storing a kernel of display information in response to the first sequence of output words, in response to the second sequence of output words, and in response to the third sequence of output words;

a kernel processor coupled to the kernel memory and generating spatially filtered display information in response to the kernel of display information stored by the kernel memory; and

a display monitor coupled to the kernel processor and generating a spatially filtered display in response to the spatially filtered display information.

--81. In an image processing system, a process comprising:

a processor generating perspective image information;

writing a sequence of input words into a first memory in response to the image information;

outputting a first sequence of output words from a second memory simultaneously with the writing of the sequence of input words into the first memory; and

outputting a second sequence of output words from a third memory simultaneously with the writing of the sequence of input words into the first memory and simultaneously with the outputting of the first sequence of output words from the second memory.

--82. In an image processing system, a process comprising:

generating antialiased image information;

generating a sequence of input words in response to the image information;

writing a sequence of input words into at least one of a plurality of memories;

accessing a sequence of words of information from each of at least two of the plurality of memories;

outputting a plurality of sequences of output words in response to the words of information accessed from the at least two of the plurality of memories;

generating a double buffer control signal; and

selecting a memory from the plurality of memories for the first buffer and selecting the at least two of the memories for the second buffer in response to the double buffer control signal.

--83. In an image processing system, a process comprising:

generating scanned out image information;

writing a sequence of input words into a first memory in a plurality of memories in response to the image information; and

outputting a first sequence of output words from a second memory in the plurality of memories, outputting a second sequence of output words from a third memory in the plurality of memories, and outputting a third sequence of output words from a forth memory in the plurality of memories simultaneously with the writing of the sequence of input words into the first memory by the input circuit.

--84. In an image processing system, a process comprising:

generating filtered image information;

storing a sequence of input words into a first memory in a plurality of memories in response to the image information;

outputting a first sequence of output words from a second memory in the plurality of memories, outputting a second sequence of output words from a third memory in the plurality of memories, and outputting a third sequence of output words from a forth memory in the plurality of memories simultaneously with the storing of the sequence of input words into the first memory by the input circuit; and

generating a filtered sequence of output words by kernel processing the first sequence of output words, the second sequence of output words, and the third sequence of output words.

--85. In an image processing system, a process comprising:

generating occulted image information;

selecting either a first memory, a second memory, or a third memory as an input memory from a plurality of memories;

storing a sequence of input words into an input memory in response to the image information;

selecting either the first memory, the second memory, or the third memory as a first output memory;

selecting either the first memory, the second memory, or the third memory as a second output memory; and

outputting a first sequence of output words from the first output memory and a second sequence of output words from the second output memory.

--86. In an image processing system, a process comprising:

generating range-related detail image information;

generating an input line of display information in response to the image information;

storing three lines of display information in response to the input line of display information; and

simultaneously generating three lines of display information in response to the three lines of double buffered display information.

--87. In an image processing system, a process comprising:

generating image information;

generating an input line of display information in response to the image information;

storing three lines of double buffered display information in response to the input line of display information; and

simultaneously generating three lines of display information in response to the three lines of double buffered display information.

--88. In an image processing system, a process comprising:

generating rotated image information;

generating an input line of display information in response to the image information;

storing three lines of double buffered display information in response to the input line of display information; and

simultaneously generating three lines of display information in response to the three lines of double buffered display information.

--89. In an image processing system, a process comprising:

generating translated image information;

generating an input line of display information in response to the image information;

storing a first line of display information in response to the input line of display information;

accessing the first line of display information;

storing a second line of display information in response to the accessed first line of display information; and

accessing the second line of display information.

--90. In an image processing system, a process comprising:

generating scaled image information;

generating an input line of display information in response to the image information;

storing a first line of display information in response to the input line of display information;

accessing the first line of display information;

storing a second line of display information in response to the accessed first line of display information;

accessing the second line of display information;

storing a third line of display information in response to the accessed second line of display information; and

accessing the third line of display information.

--91. In an image processing system, a process comprising:

generating perspective image information;

generating an input sequence of words in response to the image information;

storing a sequence of words by each of a plurality of memories;

generating a plurality of simultaneous output sequences of words;

precessing the plurality of memories between an input memory storing the input sequence of words and a plurality of output memories each generating a sequence of words simultaneously with the other output memories each generating a sequence of words.

--92. In an image processing system, a process comprising:

generating antialiased image information;

generating input words in response to the image information;

generating output words;

storing words in each of a plurality of random access memories;

generating a first address;

generating a second address;

multiplexing the first address and the second address to provide the first address to at least one of the plurality of random access memories and to provide the second address to at least one of the plurality of random access memories in response to an address control signal;

selecting at least one of the random access memories that is to receive the input words generated by the input circuit in response to an input control signal;

selecting at least one of the random access memories that is to provide the output words to the output circuit in response to an output control signal;

generating the address control signal, the input control signal, and the output control signal to select at least one input memory storing the input words and at least one output memory generating the output words.

--93. In an image processing system, a process comprising:

generating scanned out image information;

generating an input sequence of words in response to the image information;

generating a plurality of simultaneous output sequences of words;

storing a sequence of words in each of a plurality of random access memories;

generating an input address;

generating an output address;

multiplexing the input address and the output address to provide the input address to an input one of the plurality of random access memories and to provide the output address to a plurality of output ones of the plurality of random access memories in response to an address precessional control signal;

selecting the random access memory that is to receive the input sequence of words generated by the input circuit in response to an input precessional control signal;

selecting the plurality of random access memories that are to generate an output sequences of words to the output circuit in response to an output precessional control signal;

generating the address precessional control signal, the input precessional control signal, and the output precessional control signal to precess the plurality of memories between an input memory storing the input sequence of words and a plurality of output memories each generating a sequence of words simultaneously with the other output memories each generating a sequence of words.

--94. In an image processing system as set forth in claim 88, the process further comprising making a product.

--95. An image processing system comprising:

a memory storing an image;

an accessing circuit coupled to the memory and accessing the image from the memory; and

a display processor coupled to the accessing circuit and generating a rotated and translated image by rotation and translation processing of the image accessed by the accessing circuit.

--96. An image processing system comprising:

a database memory storing a database image;

an image memory storing a portion of the database image;

an image memory loading circuit coupled to the database memory and coupled to the image memory and loading a portion of the database image stored by the database memory into the image memory; and

an image processor coupled to the image memory and generating a processed image by processing the image stored in the image memory.

--97. A display system comprising:

a memory storing an image;

a display processor coupled to the memory and scanning out the image stored in the memory; and

a display medium coupled to the display processor and displaying the image scanned out by the display processor.

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Respectfully submitted,

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